REMARKS

This is a full and timely response to the outstanding final Office Action mailed September 6, 2005 (Paper No. 2). Upon entry of this response, claims 1-8, 19-25, 33-46, and 48-90 are pending in the application. In this response, claims 10-17 have been cancelled. Applicants respectfully request that the amendments being filed herewith be entered and request that there be reconsideration of all pending claims.

1. Rejection of Claims 1-8, 10-17, 19-25, 33-46, and 61-90 under 35 U.S.C. §103

Claims 1-8, 10-17, 19-25, 33-46, and 61-90 have been rejected under §103(a) as allegedly obvious over *Delvaux* (6,718,419) in view of *Delattre et al.* (6,606,302). Applicants respectfully traverse this rejection. It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly, all elements/features/steps of the claim at issue. *See, e.g., In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

A. Claims 1, 19, 33, 40, 61, 68, 76, and 84

Applicants respectfully submit that claims 1, 19, 33, 40, 61, 68, 76, and 84 are allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the feature of "wherein...at least two of the plurality of channel connections associated with the plurality of first channel ports is via no more than one of the plurality of addresses" as recited in claims 1, 19, 33, 40, 61, 68, 76, and 84.

i. The *Delvaux* Reference

The Office Action alleges that

> Delvaux discloses a plurality of physical layer devices in communication using an address line (Col. 13, line 66 to Col. 14, line 18), where it would

> have been obvious to one of ordinary skill in the art at the time of the invention that *if one address line is used for a plurality of physical layer devices communicating with an ATM layer device (Col. 13, line 66 to Col. 14, line 18), only one address is necessary to route information out of the physical layer devices*. Delvaux discloses the address line functioning as an address (Col. 14 lines 19-42).
> (Office Action, p. 17, emphasis added.)

Applicants respectfully disagree with the premise of the Office Action argument, namely, that *Delvaux* discloses that ***one address line*** is used for a plurality of physical devices. When analyzed as a whole, including the Figures, *Delvaux* clearly teaches a conventional address bus using multiple address lines, where a combination of n address lines is used to specify one of 2^n addresses. The passage cited in the Office Action specifically refers to "address lines" (plural), as does FIG. 7, which shows "TxAddr 5." Further evidence of this understanding of *Delvaux* is that FIG. 7 is described as being "in accordance with the UTOPIA interface" (Col. 14, lines 10-14), which would be understood by one skilled in the art to include an n-bit address bus specifying one of 2^n addresses.

Thus, *Delvaux* does not disclose an addressing scheme where address line 0 is associated with PHY1, address line 1 is associated with PHY2, etc., as the Office Action appears to suggest. Nor does *Delvaux* disclose any sort of multicast address scheme where the same address is decoded by multiple PHYs. Indeed, the UTOPIA interface, which FIG. 7 adheres to, does not include multicast addressing.

Since the premise of the Office Action – that *Delvaux* discloses that ***one*** address line is used for a plurality of physical devices – is faulty, Applicants submit that the conclusion of obviousness is also flawed.

ii. The *Delattre et al.* Reference

The Office Action further alleges that

> Furthermore, Delattre discloses a point to multi point configuration from a first class (class 0 in fig 5a) to a group of first output ports (see fig 5a). It would have been obvious to one of ordinary skill in the art at the time of the invention that a point to multipoint connection may use one address to access a number of connections.
> (Office Action, p. 17.)

Applicants agree that *Delattre et al.* teaches a point to multipoint configuration. However, *Delattre et al.* does not discuss any sort of addressing scheme used to implement this configuration, and therefore does not disclose, teach, or suggest "wherein...at least two of the plurality of channel connections associated with the plurality of first channel ports is via no more than one of the plurality of addresses." The Office Action statement of obviousness is merely conclusory, with no support in the record.

iii. The Combination of *Delvaux* in view of *Delattre et al.*

As discussed above, the references do not disclose, teach, or suggest, alone or in combination, at least the above-described feature recited in claims 1, 19, 33, 40, 61, 68, 76, and 84. Therefore, a *prima facie* case establishing an obviousness rejection has not been made. Thus, claims 1, 19, 33, 40, 61, 68, 76, and 84 are not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

iv. The Obviousness Rejection is Improper

The Office Action does not explicitly allege that either *Delvaux* or *Delattre et al.* discloses the above-described feature, instead alleging that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention that a point to multipoint connection may use one address to access a number of connections." (Office Action, p. 17.) Therefore, the rejection of claims 1, 19, 33, 40, 61, 68, 76, and 84 is improper and should be withdrawn.

A ***hypothetical*** allegation of obviousness which is proper, and in accordance with MPEP §706, might allege that the claims are obvious over Delvaux in view of Delattre et al., and further

in view of the knowledge of person of ordinary skill in the art that a point to multipoint connection may use one address to access a number of connections. However, to properly support this hypothetical rejection, the Examiner must also allege that the fact that "a point to multipoint connection may use one address to access a number of connections" is either well-known, or is within the personal knowledge of the Examiner.

Applicants respectfully submit that this fact is not so notoriously well-known that knowledge of it may be assumed in the absence of documentary support, since the fact is not "capable of instant and unquestionable demonstration as being well-known," as required by MPEP 2144.03. Therefore, a *prima facie* case establishing an obviousness rejection has not been made. Thus, claims 1, 19, 33, 40, 61, 68, 76, and 84 are not obvious under the proposed combination, and the rejection should be withdrawn.

In the alternative, the Examiner has not provided an affidavit stating that this fact is within his personal knowledge. Therefore, a *prima facie* case establishing an obviousness rejection has not been made. Thus, claims 1, 19, 33, 40, 61, 68, 76, and 84 are not obvious under the proposed combination, and the rejection should be withdrawn.

B. Claims 10-17

Claims 10-17 are cancelled without prejudice, waiver, or disclaimer, and the rejection of these claims is therefore rendered moot. Applicants take this action merely to reduce the number of disputed issues and to facilitate early allowance and issuance of other claims in the present application. Applicants reserve the right to pursue the subject matter of these cancelled claims in a continuing application, if Applicants so choose, and do not intend to dedicate any of the cancelled subject matter to the public. Applicants expressly reserve the right to present cancelled claims 10-17, or variants thereof, in continuing applications to be filed subsequent to the present application.

C. Claims 33, 40, and 61

Applicants respectfully submit that claim 33 is allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest the feature of "based on the VPI/VCI value and a predefined set of rules,...determine which of the plurality of addresses on the local interface to which the VPI/VCI value is associated; and where the ATM cell corresponds to the first class of service, providing the ATM cell to all of the first channel ports via a first unique address on the local interface and where the ATM cell corresponds to the second class of service, providing the ATM cell to one of the second channel ports via a second unique address."

In addition, claim 40 is allowable for at least the reason that the proposed combination does not disclose, teach, or suggest the feature of "based on the VPI/VCI value and a first predefined set of rules...determine which of a plurality of addresses on a first local interface to which the VPI/VCI value is associated; and where the ATM cell corresponds to the first class of service, providing the ATM cell to an address expansion device via a first unique address on the local interface and, based on the VPI/VCI value and a second predefined set of rules, providing the ATM cell to one of the plurality of first channel ports associated with the VPI/VCI value via one of a plurality of addresses on a second local interface connected to the address expansion device and where the ATM cell corresponds to the second class of service, providing the ATM cell to one of the second channel ports via a second unique address on the first local interface."

Furthermore, claim 61 is allowable for at least the reason that the proposed combination does not disclose, teach, or suggest the feature of "a third portion of logic for determining, based on the VPI/VCI value and a first predefined set of rules...which of a plurality of addresses on a first local interface to which the VPI/VCI value is associated; and a fourth portion of logic for (i) providing the ATM cell to an address expansion device via a first unique address on the local

interface and for providing, based on the VPI/VCI value and a second predefined set of rules, the ATM cell to one of the plurality of first channel ports associated with the VPI/VCI value via one of a plurality of addresses on a second local interface where the ATM cell corresponds to the first class of service and (ii) providing the ATM cell to one of the second channel ports via a second unique address on the first local interface where the ATM cell corresponds to the second class of service."

Delvaux discloses that ATM cells have VPI/VCI values, and that each circuit is identified by a VPI/VCI pair. (Col. 12, line 60 to Col. 3, line 35.) However, *Delvaux* does not disclose, teach, or suggest that either the ATM layer device 134 or the physical layer device 136 uses the VPI/VCI pair in order to route a cell with a certain class of service to a particular port or ports of a PHY.

Delattre et al. is directed to an ATM switch that includes multiple shapers on each input line card, where one shaper is dedicated to flows in one class of service (VBRnrt) and the remaining shapers are dedicated to another class of service (UBR/ABR). However, there is no discussion of *Delattre et al.* of how an addressing scheme between the ATM layer and the PHY layer relates to the shapers and the classes of service.

Applicant's claimed invention as defined in claims 33, 40, and 61 has a local interface with multiple addresses, and uses VPI/VCI to determine which of these addresses is associated with the VPI/VCI value. Furthermore, the local interface addressing scheme is used to provide cells with different classes of service to specific PHY ports. Specifically, cells in a first class of service are provided "to ***all*** of the first channel ports via a ***first unique address*** on the local interface," and cells in a second class of service are provided "to ***one*** of the second channel ports via a ***second unique address***."

The cited references do not disclose, teach, or suggest, alone or in combination, at least the above-described feature. Therefore, a prima facie case establishing an obviousness rejection has not been made. Thus, claims 33, 40, and 61 are not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

D. Claims 68, 76, and 84

Applicants respectfully submit that claims 68, 76, and 84 are allowable for at least the reason that the proposed combination of *Delvaux* in view of *Delattre et al.* does not disclose, teach, or suggest at least the feature of "the local interface establishing a plurality of first class connections, each first class connection being between one of the ATM communications channels and one of the first channel ports, all of the first class connections using a single address on the local interface, each second class connection being between one of the ATM communications channels and one of the second channel ports, each of the second class connections having a unique address on the local interface" as recited in claims 68, 76, and 84. In addition, the proposed combination does not disclose, teach, or suggest the feature of "the local interface and expansion interface configured to establish a first plurality of channel connections, each of the first plurality of channel connections being established between one of the first plurality of ATM communication channels and one of the first channel ports, and the local interface and expansion interface further configured to establish a second plurality of channel connections, each of the second plurality of channel connections being established between one of the second plurality of ATM communication channels and one of the second channel ports" as recited in claim 76.

FIG. 8 of *Delvaux* teaches a bus extender for the UTOPIA bus which extends the number of PHYs supported from 16 to 32 without modifying the PHY layer devices. (Col. 14, line 55 to Col. 5, line 60.) The addressing scheme used by the bus extender is as follows. Six address bits

are provided to the ATM layer device 134. (Col. 15, lines 1-5.) A range select decoder 162 uses the two most significant address bits to select one of four sets of PHYs. (Col. 15, lines 15-35.) The lowest four address bits are used to select one of the 16 PHYs within that group. (Col. 5, lines 45-55.) Thus, *Delvaux* discloses that an ATM layer device accesses each PHY by its own corresponding 6 bit address.

Delvaux does not disclose, teach, or suggest that each PHY has two ports, nor that each of the ports is associated with a class of service. *Delattre et al.* discloses an ATM switch that includes multiple shapers on each input line card, where one shaper is dedicated to flows in one class of service (VBRnrt) and the remaining shapers are dedicated to another class of service (UBR/ABR). *Delattre et al.* further suggests that cells from one shaper are output to a group of output ports. However, *Delattre et al.* does not use an addressing scheme between the ATM layer and the PHY layer to accomplish the delivery of cells from a shaper to a group of output ports. Thus, it is not clear how the class-specific shapers of *Delattre et al.* can be combined with the addressing scheme of *Delvaux* to result in the above-described features recited in claims 68, 76, and 84.

In contrast, Applicants' claimed invention as defined in claims 68, 76, and 84 uses a local interface to establish two sets of connections between an ATM layer device and the PHYs. Connections in the first set exist between one ATM channel on the ATM layer device and the PHY port associated with one class of service. Importantly, each connection in this first set uses the ***same single address*** on the local interface. Connections in the second set exist between one ATM channel on the ATM layer device and another PHY port associated with another class of service. Importantly, each connection in this second set has ***its own address*** on the local interface.

Since the references do not disclose, teach, or suggest, alone or in combination, at least the above-described features recited in claims 68, 76, and 84, a prima facie case establishing an obviousness rejection has not been made. Thus, claims 68, 76, and 84. are not obvious under the proposed combination of *Delvaux* in view of *Delattre et al.*, and the rejection should be withdrawn.

E. Claims 2-8, 11-17, 20-25, 34-39, 41-45, 61-17, 69-75, and 79-83

Since claims 1-8, 10-17, 19-25, 33-46, and 61-90 are allowable, Applicants respectfully submit that claims 2-8, 11-17, 20-25, 34-39, 41-45, 61-17, 69-75, and 79-83 are is allowable for at least the reason that each depends from an allowable claim. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). Therefore, Applicants respectfully request that the rejection of claims 2-8, 11-17, 20-25, 34-39, 41-45, 61-17, 69-75, and 79-83 be withdrawn.

CONCLUSION

Applicants respectfully request that all outstanding objections and rejections be withdrawn and that this application and presently pending claims 1-8, 19-25, 33-46, and 48-90 be allowed to issue. If the Examiner has any questions or comments regarding Applicants' response, the Examiner is encouraged to telephone Applicants' undersigned counsel.

Respectfully submitted,

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